WHAT IS CLAIMED IS:

1. An array substrate for use in a liquid crystal display device comprising:

a plurality of gate lines on a substrate;

a plurality of data lines over the substrate, each data line being perpendicular to each gate line, wherein a plurality of pixel regions are defined by the data and gate lines;

a common line on the substrate in a respective pixel region, the common line being parallel with and spaced apart from the gate line;

a plurality of common electrodes in the respective pixel region extended from the common line and elongated along a respective data line defining the respective pixel region, wherein each common electrode has a plurality of bend portions, and wherein each common electrode has a substantially sawtooth-shaped base in a region where each common electrode intersects the common line at an obtuse angle with the common line;

a plurality of pixel electrodes in the respective pixel region spaced apart from and elongated along the said common electrodes, wherein each pixel electrode has a plurality of bend portions and corresponds to each common electrode;

a connecting line in the respective pixel region contacting one end of each pixel electrode, the connecting line electrically connecting said pixel electrodes;

a switching element in the respective pixel region electrically connected with a respective gate line defining the respective pixel region and the respective data line, the switching element supplying voltage to the said pixel electrodes.

2. The array substrate according to claim 1, wherein each pixel electrode has a substantially sawtooth-shaped base in an area where each pixel electrode meets the connecting line.

3. The array substrate according to claim 2, wherein the substantially sawtooth-shaped base of each respective pixel electrode forms an obtuse angle with the connecting line.

4. The array substrate according to claim 1, wherein the connecting line in the respective pixel region overlaps a portion of the respective gate line.

5. The array substrate according to claim 4, wherein the connecting line and the respective gate line comprise a storage capacitor.

6. The array substrate according to claim 1, wherein one of the common electrodes elongates along the respective data line and electrically communicates with adjacent pixel regions.

7. The array substrate according to claim 1, wherein the common line crosses the one of bend portions of each common electrode and electrically connects a plurality of the common electrodes.

8. The array substrate according to claim 7, wherein the common line elongates along the respective gate line and communicates with other common lines in the adjacent pixel regions.

9. An array substrate for use in a liquid crystal display device comprising:

a gate line on a substrate;

a data line over the substrate, the data line being perpendicular to the gate line, wherein a plurality of pixel regions are defined by the data and gate lines;

a common line in a respective pixel region being substantially parallel with and spaced apart from the gate line;

a plurality of common electrodes in the respective pixel region extended from the common line, wherein each common electrode has a substantially zigzag shape and a substantially sawtooth-shaped base, and wherein each common line forms an angle of greater than 90° with the substantially sawtooth-shaped base;

a connecting line in the respective pixel region being parallel with a respective gate line defining the respective pixel region;

a plurality of pixel electrodes in the respective pixel region extended from the connecting line, wherein each pixel electrode has a substantially zigzag shape and a substantially sawtooth-shaped base, and wherein the common line forms an angle of greater than 90° with the sawtooth-shaped base of at least one of the pixel electrodes; and

a switching element electrically connected with the respective gate and a data line defining the respective pixel region, the switching element supplying voltage to the said pixel electrodes.

10. The array substrate according to claim 9, wherein the switching element is located in the crossing of the respective gate line and the respective data line.

11. The array substrate according to claim 10, wherein the switching element includes a source electrode that extends from the respective data line; a gate electrode that

extends from the respective gate line; a drain electrode that contacts one of the pixel electrodes through a drain contact hole; an active layer over the gate electrode and between the source and drain electrodes; and ohmic contact layers between the active layer and the source and drain electrodes.

12. The array substrate according to claim 11, wherein one of the pixel electrodes has a bend end portion over the drain electrode.

13. The array substrate according to claim 12, wherein the bend end portion overlaps a portion of the drain electrode and contacts the drain electrode through the drain contact hole

14. The array substrate according to claim 9, wherein the connecting line overlaps a portion of the respective gate line, and the connecting line and the gate line form a storage capacitor.

15. The array substrate according to claim 9, wherein a plurality of the pixel electrodes and the connecting line are made of a transparent conductive material.

16. The array substrate according to claim 9, wherein a plurality of the pixel electrodes and the connecting line are made of an opaque metallic material.

17. The array substrate according to claim 9, wherein a plurality of the common electrodes and the common line are made of a transparent conductive material.

18. The array substrate according to claim 9, wherein a plurality of the common electrodes and the common line are made of an opaque metallic material.

19. An array substrate for use in a liquid crystal display device comprising:

a gate line on a substrate;

a data line over the substrate, the data line being perpendicular to the gate line, wherein each pair of gate and data lines defines a pixel area;

a common line being parallel with and spaced apart from the gate line, wherein the common line is located in any region of the pixel area and elongates along the gate line;

a plurality of common electrodes extended from the common line, wherein each common electrode has a substantially zigzag shape and a substantially sawtooth-shaped base in a intersection where each common electrode crosses the common line, wherein each common line forms an angle of greater than 90° with the sawtooth-shaped base, and wherein one of the common electrodes elongates along the data line;

a connecting line being parallel with the gate line;

a plurality of pixel electrodes extended from the connecting line, wherein each pixel electrode has a substantially zigzag shape and a substantially sawtooth-shaped base, and wherein each common line forms an angle of greater than 90° with the substantially sawtooth-shaped base; and

a switching element electrically connected with the gate and data lines, the switching element supplying voltage to the said pixel electrodes.

20. The array substrate according to claim 19, wherein one of the pixel

electrodes has a sharply bend end portion over the switching element.

21. The array substrate according to claim 20, wherein the switching element is located in the crossing of the gate and data lines.

22. The array substrate according to claim 21, wherein the switching element includes a source electrode that extends from the data line; a gate electrode that extends from the gate line; a drain electrode that is the bend end portion of one pixel electrode; an active layer over the gate electrode and between the source and drain electrodes; and ohmic contact layers between the active layer and the source and drain electrodes.

23. The array substrate according to claim 22, wherein the drain electrode and the pixel electrodes are separately formed on different layers.

24. The array substrate according to claim 22, wherein the data line, the connecting line, the pixel electrodes, and the source and drain electrodes are made of the same material.

25. The array substrate according to claim 22, wherein a substance of the drain electrode is different from that of the pixel electrodes.

26. The array substrate according to claim 19, wherein the connecting line overlaps a portion of the gate line, and the connecting line and the gate line form a storage capacitor.

27. The array substrate according to claim 19, wherein the common line and each common electrode intersect in one bend portion of each common electrode.

28. The array substrate according to claim 19, wherein the common line is connected with other common lines in adjacent pixel areas in order to form a mesh shape.

29. The array substrate according to claim 19, wherein one of the common electrodes is connected with other common electrodes that are positioned in adjacent pixel areas in order to form the mesh shape.

30. The array substrate according to claim 19, wherein a plurality of the pixel electrodes and the connecting line are made of a transparent conductive material.

31. The array substrate according to claim 19, wherein a plurality of the pixel electrodes and the connecting line are made of an opaque metallic material.

32. The array substrate according to claim 19, wherein a plurality of the common electrodes and the common line are made of a transparent conductive material.

33. The array substrate according to claim 19, wherein a plurality of the common electrodes and the common line are made of an opaque metallic material.